REMARKS

Upon entry of this amendment, which amends claim 1 and cancels claims 15-18, claims 1-14 and 19-23 are pending in the present application. Applicants reserve the right to file claims 15-18 in a separate application.

Applicants note that claim 1 was amended to correct a typographical error. Specifically, the word "to" was deleted.

Claims 1-14 and 19-23 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Lu et al. (U.S. Pat. No. 5,943,581, hereinafter "Lu") in view of Michaelis (U.S. Pat. No. 6,156,606) and further in view of Ballantine et al. (U.S. Pat. No 6,271,100, hereinafter "Ballantine").

As best understood, the rejection asserts that Lu discloses all claimed subject matter, but fails to expressly disclose the exposed sidewall surfaces of the trench are annealed in a hydrogen ambient environment. Michaelis is cited as disclosing the step of annealing the sidewall surfaces of the trench using hydrogen gas at temperatures of between 600-800 °C to remove any native oxide from the side wall surfaces, expose the bare silicon of the substrate, and obtain a rutile crystal structure. Further, the rejection asserts that Ballantine discloses the step of annealing the sidewall surfaces of the trench using a hydrogen gas at the temperatures of between 900-1000 °C at about a pressure of 100 Torr or less to substantially reduce stress at corner regions that exist between the trench and the substrate. The rejection then asserts that it would have been obvious in view of Lu, Michaelis, and Ballantine to anneal the trench to reduce the number of defects in the trench created during the step of forming, and to round the corners at the open and closed ends of the trench.

Applicants respectfully submit that Lu and Michaelis, either alone or in combination, disclose or suggest every element of claims 1-14 and 19-23. For example, in amended claim 1, "annealing the trench to: (1) reduce the number of defects in the trench created during the step of forming, and (2) round corners at the open and closed ends of the trench" is not disclosed or suggested. Additionally, independent claims 6, 9, and 19 include either one or both of the above elements.

Also, applicants respectfully submit that Ballantine does not qualify as prior art under the provisions of 35 U.S.C. §103. Ballantine was filed on Feb. 24, 2000. The present application was filed on Nov. 24, 1999. Ballantine was filed after the filing date of the present application and thus, applicants respectfully submit that Ballantine is not prior art.

Accordingly, in view of Ballantine not being prior art, applicants respectfully submit that Lu and Michaelis do not disclose or suggest every element of claims 1, 6, 9, and 19.

Claims 2-5, 7-8, 10-14, and 20-23 depend from independent claims 1, 6, 9, and 19 and thus, derive patentability at least therefrom. Accordingly, applicants respectfully request withdrawal of the rejections.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

12/21/01
Date

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A method of forming a trench in a semiconductor substrate, the trench defined by an open end at a major surface of the substrate and a closed end within the body of the substrate, the method comprising the steps of:

(a) forming a trench that extends a predetermined distance into the substrate; and

(b) annealing the trench to:

(1) reduce the number of defects in the trench created during the step of forming, and

(2) ~~to~~ round corners at the open and closed ends of the trench.

2. The method of claim 1, wherein the step of annealing is performed using hydrogen gas.

3. The method of claim 2, wherein the step of annealing is performed within a temperature range of about 960 to 1160°C and within a pressure range of about 40 to 240 Torr.

4. The method of claim 1, wherein the step of forming the trench, is performed using an anisotropic etch.

5. The method of claim 4, wherein following the annealing step, the width of the trench away from the rounded ends, remains substantially the same as the width prior to the annealing step.

6. A method of forming a trench in a semiconductor substrate, the trench defined by an open end at a major surface of the substrate and by a closed end within the body of the substrate, the method comprising the steps of:

(a) providing a substrate;

(b) growing a masking layer on the major surface of the substrate;

(c) selectively etching, through the masking layer to the major surface of the substrate, to define a trench opening access;

(d) anisotropically etching, from the trench opening access and into the body of the substrate to form a trench;

(e) removing the selectively etched masking layer; and

(f) annealing the trench so that corners at the open and closed ends of the trench become rounded.

7. The method of claim 6, wherein the step of annealing is performed using hydrogen gas.

8. The method of claim 7, wherein the step of annealing is performed within a temperature range of about 960 to 1160°C and within a pressure range of about 40 to 240 Torr.

9. A method of forming a trench in an epitaxial layer of a semiconductor substrate, the trench defined by a closed end at a major surface of the epitaxial layer and a closed end within the body of the epitaxial layer, the method comprising the steps of:

(a) forming a trench that extends a predetermined distance into the epitaxial layer; and

(b) annealing the trench so that corners at the open and closed ends of the trench become rounded.

10. The method of claim 9, wherein the step of annealing is performed using hydrogen gas.

11. The method of claim 10, wherein the step of annealing is performed within a temperature range of about 960 to 1160°C and within a pressure range of about 40 to 240 Torr.

12. The method of claim 9, wherein the step of annealing also functions to reduce the number of material defects in and/or on the walls of the trench.

13. The method of claim 9, wherein the step of forming the trench is performed using an anisotropic etch.

14. The method of claim 13, wherein, following the annealing step, the width of the trench, away from the rounded ends, remains substantially the same as the width prior to the annealing step.

15-18. (Canceled).

19. A method of making a trench field effect transistor, comprising:

(a) providing a semiconductor substrate of a first dopant charge type, the substrate embodying the drain of the trench field effect transistor;

(b) growing an epitaxial layer of the same first dopant charge type on the substrate, the epitaxial layer having a different resistivity than the resistivity of the substrate;

(c) forming at least one trench into the epitaxial layer, each trench defined by a first end in a plane defined by a major surface of the substrate and by walls that extend to a second end at a predetermined depth into the epitaxial layer;

(d) annealing the at least one trench to:

(1) reduce the number of defects in the at least one trench created during the step of forming the at least one trench, and

(2) round corners at the first and second ends of the at least one trench;

(e) growing a dielectric layer on the walls of the at least one trench;

(f) forming a conductor over the dielectric layer, the conductor embodying the gate of the trench field effect transistor;

(g) patterning the epitaxial layer and implanting a dopant of a second charge type to form wells interposed between adjacent trenches; and

(h) patterning the epitaxial layer and implanting a dopant of the first charge type to form regions that embody the source regions of the field effect transistor.

20. The method of claim 19, further including the step of forming one or more heavy bodies of the second charge type positioned above the wells and between the source regions, each heavy body forming an abrupt junction with its corresponding well.

21. The method of claim 19, wherein the step of annealing is performed using hydrogen gas.

22. The method of claim 21, wherein the step of annealing is performed within a temperature range of about 960 to 1160°C and within a pressure range of about 40 to 240 Torr.

23. The method of claim 19, wherein the step of forming the at least one trench is performed using an anisotropic etch.